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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/737,191	12/15/2003	Kimmo Mylly	915-007.68	5502
4955 7590 06/25/2008 WARE FRESSOLA VAN DER SLUYS & ADOLPHSON, LLP BRADFORD GREEN, BUILDING 5 755 MAIN STREET, P O BOX 224 MONROE, CT 06468				
EXAMINER FRANKLIN, RICHARD B				
ART UNIT 2181		PAPER NUMBER		
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/737,191

Applicant(s)

MYLLY ET AL.

Examiner

RICHARD FRANKLIN

Art Unit

2181

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 March 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4, 6-11, 13, 14 and 16-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 11, 13 and 17-20 is/are allowed.
- 6) ☒ Claim(s) 1-4, 6-10, 14 and 16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB08)
- Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

1. Claims 1 – 4, 6 – 11, 13 – 14, and 16 – 20 are pending.

Response to Arguments

2. Applicant's arguments filed 26 March 2008 have been fully considered but they are not persuasive.

Applicant has argued that the relied upon reference, US Patent Application Publication No. 2003/0212857 (hereinafter Pacheco), does not teach determining when at least one of the at least two peripheral devices is ready for operation after completion of the initialization of each of the at least two peripheral devices, and electrically combining information indicative of a time required for an initialization of a respective one of at least two peripheral devices, as required by claim 1. However, the Examiner respectfully disagrees. The Examiner believes there could be two interpretations of the language present in claim 1. Claim 1 recites in part:

using said combined information for determining when at least one of the at least two peripheral devices is ready for operation after completion of an initialization of each of said at least two peripheral devices.

In the first interpretation, the combined information is used in a determination performed after completion of an initialization of each of peripherals to determine when one of the peripherals is ready for operation. Using this interpretation, the determining step is performed only after each peripheral device has completed initialization. The

Examiner believes this is the interpretation the Applicant has taken on pages 2 and 3 of the response filed 26 March 2008.

In the second interpretation, the combined information is used to determine when a peripheral is ready for operation after it has completed initialization. Using this interpretation, the determining step is performed at any time, and is used to determine when the peripheral device is ready to operate after it has completed initialization. This is the interpretation the Examiner has taken in interpreting the claim language. Pacheco teaches using the combined information to determine when each group of disks has "spun up." Pacheco has defined the term "spun up" as "the time required to perform the requisite power-on sequence (sometimes referred to as boot time)" (Pacheco; Paragraph [0007] Lines 3 – 6). Microsoft Computer Dictionary 5th Edition (Copyright 2002; Microsoft Press) defines the term "boot" as:

boot¹ *n.* The process of starting or resetting a computer. When first turned on (cold boot) or reset (warm boot), the computer executes the software that loads and starts the computer's more complicated operating system and prepares it for use.

Therefore, once a disk has completed "spinning up" it is ready for operation because it has gone through the boot process. The determination performed by Pacheco to determine when to start "spinning up" the next group of drives based on the completion of a previous set of drives therefore is also a determination of when the previous set of drives is ready for operation.

Applicant has also argued that "the bus of Pacheco does not perform electrical combining, as recited in claim 1" in lines 15 and 16 on page 3 of the response filed 26 March 2003. However, the Examiner notes that claim one has no mention of a bus or specific structure that performs the electrical combining. Furthermore, Applicant goes on to admit that "the combination, which is for determining an activation sequence, is then performed by an activation sequence timing schedule program" in lines 20 and 21 on page 3 of the response filed 26 March 2003. Since claim 1 does not recite a specific structure in which the combination is performed, the combination performed in Pacheco is sufficient to anticipate the combination of the claim. The Examiner notes however, that claims 11 and 13 do recite that a bus performs the electrical combination, in which Pacheco is silent.

Applicant has also argued, regarding claim 16, that one of ordinary skill in the art would not come to the idea of operating the SCSI devices of Pacheco according to an open drain mode bus protocol, because such a teaching would not fit to the described approach. However, the Examiner respectfully disagrees. The SCSI devices and the SCSI bus of Pacheco perform in a mode in which each device transmits data sequentially over the bus. However, US Patent No. 6,233,625 (hereinafter Vander Kamp) teaches that SCSI devices can operate according to "well-known" SCSI-I or SCSI-II bus protocols (Vander Kamp; Col 5 Lines 39 – 40). Since SCSI-I is an open drain mode bus protocol that is "well known" in the operation of SCSI devices, it would have been obvious to one of ordinary skill that the teachings of Pacheco could be

modified to utilize the open drain mode bus protocol instead of the protocol taught by Pacheco.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 – 3, and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Application Publication No. 2003/0212857 (hereinafter Pacheco).

As per claim 1, Pacheco teaches a method comprising transmitting information (Figure 5B "BYTE 4-5 and 6-7") indicative of a time required for an initialization of a respective one of at least two peripheral devices (Figure 2 Items 222, and 226a – 226n) from each of the at least two peripheral devices (Paragraph [0040] Lines 12 – 15); electrically combining the information from each of the at least two peripheral devices to produce combined information indicating a time which is required at the most by any of the at least two peripheral devices for its respective initialization (Figure 8A "Max Spin-Up Period", Paragraph [0047] Lines 4 – 7, See "Response to Arguments" presented above); and using the combined information for determining when at least one of the at least two peripheral devices is ready for operation after completion of an initialization of

each of the at least two peripheral devices (Paragraph [0049] Lines 25 – 28 [Based on the startup times, the system determines when a group of drives has spun-up and is initialized and is ready to move onto the next group of drives], See “Response to Arguments” presented above).

As per claim 2, Pacheco also teaches wherein the information indicative of the time required for the initialization of the respective one of the at least two peripheral devices is an information indicative of the time required for the initialization of the respective one of the at least two peripheral devices at a maximum under regular circumstances (Figure 5B “BYTE 4-5, Typical Start Time (ms)”, Paragraph [0034] Lines 7 – 9).

As per claim 3, Pacheco also teaches wherein at least one of the at least two peripheral devices transmits the information to the host device upon a predetermined command received from the host device (Figure 5A Item 500, Paragraph [0040] and Paragraph [0044] Lines 12 – 24).

As per claim 14, Pacheco teaches a computer program product comprising a computer readable storage structure embodying computer program code thereon for execution by a computer processor, wherein the computer program code comprises instructions for performing a method comprising receiving combined information indicating a time which is required at the most be any of at least two peripheral devices

(Figure 2 Items 226a – 226n) for its respective initialization (Figure 8A "Max Spin-Up Period", Paragraph [0047] Lines 4 – 7); and using the combined information for determining when at least one of the at least two peripheral devices is ready for operation after completion of an initialization of each of the at least two peripheral devices (Paragraph [0049] Lines 25 – 28 [Based on the startup times, the system determines when a group of drives has spun-up and is initialized and is ready to move onto the next group of drives], See "Response to Arguments" presented above).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication No. 2003/0212857 (hereinafter Pacheco) in view of US Patent No. 5,566,351 (hereinafter Crittenden).

As per claim 4, Pacheco teaches the method as described per claim 1 (See rejection of claim 1 above).

Pacheco does not teach wherein the host device uses the common initialization timeout value for adapting a polling frequency which is to be employed for polling the at least one of the at least two peripheral devices on whether the at least one peripheral device has completed its respective initialization.

However, Crittenden teaches wherein the host device uses the common initialization timeout value for adapting a polling frequency which is to be employed for polling the at least one of the at least two peripheral devices on whether the at least one peripheral device has completed its respective initialization (Crittenden; Col 5 Lines 14 – 21).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Pacheco to include the adaptive polling frequency because doing so allows for the system to maximize data throughput by not permitting excessive sleep periods and simultaneously minimize central processing (CPU) load by avoiding excessive polling (Crittenden; Col 5 Lines 26 – 29).

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication No. 2003/0212857 (hereinafter Pacheco) in view of US Patent No. 6,964,018 (hereinafter Masui).

As per claim 6, Pacheco teaches the method as described per claim 1 using SCSI devices (See rejection of claim 1 above).

Pacheco does not teach wherein one of the peripheral devices is a memory card.

However, Masui teaches wherein a SCSI device could be a memory card (Masui; Col 13 Lines 41 – 44).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Pacheco to include the

memory card because memory cards are an example of a storage device that can be connected to a SCSI bus (Masui; Col 13 Lines 41 – 44).

6. Claims 7 – 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication No. 2003/0212857 (hereinafter Pacheco) in view of US Patent No. 6,964,018 (hereinafter Masui) and further in view of The MultiMediaCard System Specification Version 3.31 by the MMCA Technical Committee (hereinafter MMCA).

As per claims 7 – 10, Pacheco in combination with Masui teach the use of the method of claim 1 with a memory card.

Pacheco in combination with Masui does not teach wherein the memory card is a MultiMediaCard™ (MMC) system or implements MMC functions.

However, MMCA teaches the use of a MMC as a storage device (MMCA; Page 11 Paragraph 1); the peripheral devices transmit the information to the host device upon receipt of a CMD1 command from the host device (MMCA; Page 81 Section 6.3 Power Up); the peripheral devices retrieve the information from an operating condition register (OCR) of the peripheral devices (MMCA; Page 67 Section 5.1 OCR Register); and the peripheral devices transmit the information in an R3 response to the host device (MMCA; Pages 53 – 55 Section 4.9 Responses).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings Pacheco in combination

with Masui because the use of the MMC system allows for low costs data storage that covers a large area of applications (MMCA; Page 11 Paragraph 1).

7. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication No. 2003/0212857 (hereinafter Pacheco) in view of US Patent No. 6,233,625 (hereinafter Vander Kamp).

As per claim 16, Pacheco teaches the method as described per claim 1 using SCSI devices and a SCSI bus (See rejection of claim 1 above)

Pacheco does not explicitly teach wherein transmitting information indicative of the time required for an initialization of a respective one of the at least two peripheral devices from each of the at least two peripheral devices via a bus to the host device is performed in an open drain mode of the bus.

However, Vander Kamp teaches that SCSI devices operate according to the SCSI-I or SCSI-II bus protocols (Vander Kamp; Col 5 Lines 39 – 40). The SCSI-I bus protocol is an open drain mode bus protocol.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings Pacheco to include the open drain mode because doing so is well known when using SCSI devices (Vander Kamp; Col 5 Lines 39 – 40, See "Response to Arguments" presented above).

Allowable Subject Matter

8. Claims 11, 13, and 17 – 20 are allowed.
9. The following is an examiner's statement of reasons for allowance:

Claims 11, 13, 17, and 19 are allowable because the prior art of record fails to teach or suggest alone or in combination ***a bus configured to electrically combine information indicative of a time required for an initialization of a respective one of at least two peripheral devices to produce combined information indicating a time which is required at the most by any of the at least two peripheral devices for its respective initialization***, as required by independent claim 11, ***in combination with the other recited claim limitations*** (emphasis added). Support for this limitation can be found in the originally filed specification on Page 19 Lines 10 – 21. The prior art of record teaches a bus (Pacheco; Figure 2 Item 202) and combined information (Pacheco; Figure 8A "Max Spin-Up Period," Paragraph [0047] Lines 4 – 7), but does not teach that the bus combines the information indicative of a time required for an initialization of a respective one of at least two peripheral devices in order to produce the combined information.

Claims 18 and 20 are allowable because of their dependency upon allowable claims 17 and 19 indicated above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **RICHARD FRANKLIN** whose telephone number is (571)272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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